

NL17SZ74

Single D Flip Flop

The NL17SZ74 is a high performance, full function Edge triggered D Flip Flop, with all the features of a standard logic device such as the 74LCX74.

Features

- Extremely High Speed: t_{PD} 2.6 ns (typical) at $V_{CC} = 5.0$ V
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- 5.0 V Tolerant Inputs – Interface Capability with 5.0 V TTL Logic
- LVTTL Compatible
- LVCMOS Compatible
- 24 mA Balanced Output Sink and Source Capability
- Near Zero Static Supply Current (10 μ A) Substantially Reduces System Power Requirements
- Replacement for NC7SZ74
- Tiny Ultra Small Package Only 2.1 X 3.0 mm
- High ESD Ratings: 2000 V Human Body Model
200 V Machine Model
- Chip Complexity: FET = 64
- Pb-Free Packages are Available

TRUTH TABLE

Inputs				Outputs		Operating Mode
PR	CLR	CP	D	Q	\bar{Q}	
L	H	X	X	H	L	Asynchronous Set Asynchronous Clear Undetermined
H	L	X	X	L	H	
L	L	X	X	H	H	
H	H	\uparrow	h	H	L	Load and Read Register
H	H	\uparrow	l	L	H	
H	H	∇	X	NC	NC	Hold

- H = High Voltage Level
h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
L = Low Voltage Level
l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition
NC = No Change
X = High or Low Voltage Level and Transitions are Acceptable
 \uparrow = Low-to-High Transition
 ∇ = Not a Low-to-High Transition
For I_{CC} reasons, DO NOT FLOAT Inputs



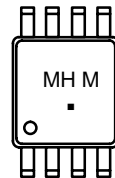
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM

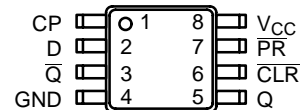


US8
US SUFFIX
CASE 493

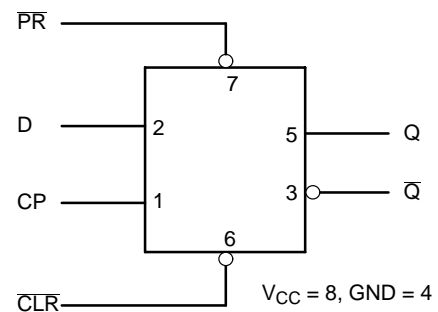


- M = Date Code
■ = Pb-Free Package

PINOUT DIAGRAM



LOGIC DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

NL17SZ74

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage – Output in High or Low State (Note 1)	-0.5 to V _{CC} +0.5	V
I _{IK}	DC Input Diode Current V _I < GND	-50	mA
I _{OK}	DC Output Diode Current V _O < GND	-50	mA
I _O	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current Per Supply Pin	±100	mA
I _{GND}	DC Ground Current Per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C
T _J	Junction Temperature Under Bias	+150	°C
θ _{JA}	Thermal Resistance (Note 2)	250	°C/W
P _D	Power Dissipation in Still Air at 85°C	250	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 3) Machine Model (Note 4) Charged Device Model (Note 5)	>2000 >200 N/A	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. I_O absolute maximum rating must be observed.
2. Measured with minimum pad spacing on an FR4 board, using 10 mm X 1 inch, 2 ounce copper trace with no air flow.
3. Tested to EIA/JESD22-A114-A.
4. Tested to EIA/JESD22-A115-A.
5. Tested to JESD22-C101-A.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _I	Input Voltage (Note 6)	0	5.5	V
V _O	Output Voltage (HIGH or LOW State)	0	V _{CC}	V
T _A	Operating Free-Air Temperature	-40	+85	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 2.5 V ±0.2 V V _{CC} = 3.0 V ±0.3 V V _{CC} = 5.0 V ±0.5 V	0 0 0	20 10 5.0	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high-logic voltage level or a low-logic input voltage level.

ORDERING INFORMATION

Device	Package	Shipping†
NL17SZ74US	US8	3000 / Tape & Reel
NL17SZ74USG	US8 (Pb-Free)	3000 / Tape & Reel
TNL17SZ74USG	US8 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NL17SZ74

DETAILED DEVICE ORDERING INFORMATION

Device Order Number	Device Nomenclature						Package Type	Tape and Reel Size
	Logic Circuit Indicator	No. of Gates per Package	Temp Range Identifier	Technology	Device Function	Package Suffix		
NL17SZ74US	NL	1	7	SZ	74	US	US8	178 mm, 3000 Unit

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	V _{CC} (V)	T _A = 25°C			-40°C ≤ T _A ≤ 85°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	High-Level Input Voltage		1.65	0.75 V _{CC}			0.75 V _{CC}		V
			2.3 to 5.5	0.7 V _{CC}			0.7 V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65			0.25 V _{CC}		0.25 V _{CC}	V
			2.3 to 5.5			0.3 V _{CC}		0.3 V _{CC}	
V _{OH}	High-Level Output Voltage V _{IN} = V _{IL} or V _{IL}	I _{OH} = 100 μA	1.65 to 5.5	V _{CC} - 0.1	V _{CC}		V _{CC} - 0.1		V
		I _{OH} = -3 mA	1.65	1.29	1.52	1.29			
		I _{OH} = -8 mA	2.3	1.9	2.1	1.9			
		I _{OH} = -12 mA	2.7	2.2	2.4	2.2			
		I _{OH} = -16 mA	3.0	2.4	2.7	2.4			
		I _{OH} = -24 mA	3.0	2.3	2.5	2.3			
		I _{OH} = -32 mA	4.5	3.8	4.0	3.8			
V _{OL}	Low-Level Output Voltage V _{IN} = V _{IH}	I _{OL} = 100 μA	1.65 to 5.5		0.008	0.1		0.1	V
		I _{OL} = 3 mA	1.65		0.10	0.24		0.24	
		I _{OL} = 8 mA	2.3		0.12	0.3		0.3	
		I _{OL} = 12 mA	2.7		0.15	0.4		0.4	
		I _{OL} = 16 mA	3.0		0.19	0.4		0.4	
		I _{OL} = 24 mA	3.0		0.30	0.55		0.55	
		I _{OL} = 32 mA	4.5		0.30	0.55		0.55	
I _{IN}	Input Leakage Current	V _{IN} = V _{CC} or GND	5.5			±0.1		±1.0	μA
I _{OFF}	Power off Input Leakage Current	5.5V or V _{IN} = GND	0			1.0		10	μA
I _{CC}	Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5			1.0		10	μA

NL17SZ74

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	V _{CC} (V)	Test Conditions	T _A = 25°C			T _A = -40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency (50% Duty Cycle) (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	75			75		MHz
		2.5 ± 0.2		150			150		
		3.3 ± 0.3		200			200		
		5.0 ± 0.5	250			250			
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	175			175		
		5.0 ± 0.5		200			200		
t _{PLH} , t _{PHL}	Propagation Delay, CP to Q or \bar{Q} (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	2.5	6.5	12.5	2.5	13	ns
		2.5 ± 0.2		1.5	3.8	7.5	1.5	8.0	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5	0.8	2.2	4.5	0.8	5.0		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t _{PLH} , t _{PHL}	Propagation Delay, PR or CLR to Q or \bar{Q} (Waveform 2)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	2.5	6.5	14	2.5	14.5	ns
		2.5 ± 0.2		1.5	3.8	9.0	1.5	9.5	
		3.3 ± 0.3		1.0	2.8	6.5	1.0	7.0	
		5.0 ± 0.5	0.8	2.2	5.0	0.8	5.5		
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	1.0	3.4	7.0	1.0	7.5	
		5.0 ± 0.5		1.0	2.6	5.0	1.0	5.5	
t _S	Setup Time, D to CP (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	6.5			6.5		ns
		2.5 ± 0.2		3.5			3.5		
		3.3 ± 0.3		2.0			2.0		
		5.0 ± 0.5	1.5			1.5			
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	2.0			2.0		
		5.0 ± 0.5		1.5			1.5		
t _H	Hold Time, D to CP (Waveform 1)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	0.5			0.5		ns
		2.5 ± 0.2		0.5			0.5		
		3.3 ± 0.3		0.5			0.5		
		5.0 ± 0.5	0.5			0.5			
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	0.5			0.5		
		5.0 ± 0.5		0.5			0.5		
t _W	Pulse Width, CP, \bar{C} LR, PR (Waveform 3)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	6.0			6.0		ns
		2.5 ± 0.2		4.0			4.0		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5	2.0			2.0			
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0		
		5.0 ± 0.5		2.0			2.0		
t _{REC}	Recover Time PR; CLR to CP (Waveform 3)	1.8 ± 0.15	C _L = 15 pF R _D = 1 MΩ S ₁ = Open	8.0			8.0		MHz
		2.5 ± 0.2		4.5			4.5		
		3.3 ± 0.3		3.0			3.0		
		5.0 ± 0.5	3.0			3.0			
		3.3 ± 0.3	C _L = 50 pF, R _D = 500 Ω, S ₁ = Open	3.0			3.0		
		5.0 ± 0.5		3.0			3.0		

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}/2 (per flip-flop). C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

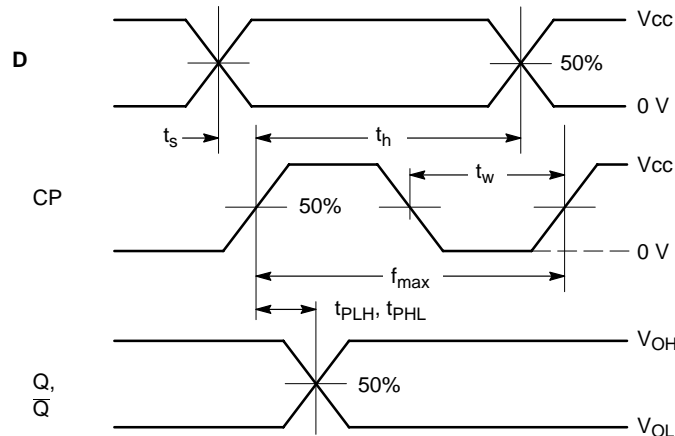
CAPACITANCE (Note 8)

Symbol	Parameter	Condition	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = 5.5 V	7.0	pF
C _{OUT}	Output Capacitance	V _{CC} = 5.5 V	7.0	pF
C _{PD}	Power Dissipation Capacitance (Note 9) Frequency = 10 MHz	V _{CC} = 3.3 V	16	pF
		V _{CC} = 5.0 V	21	

8. T_A = +25°C, f = 1 MHz

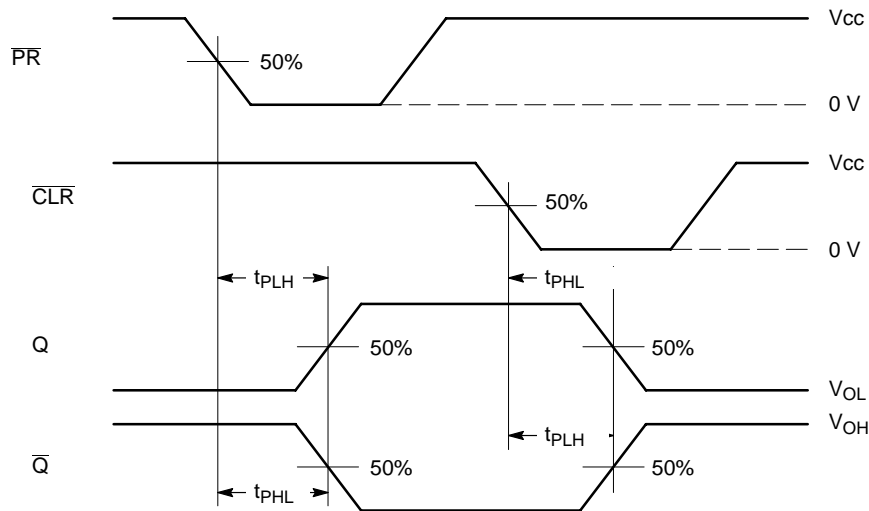
9. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (See Figure 1) C_{PD} is related to I_{CCD} dynamic operating current by the expression: I_{CCD} = C_{PD} • V_{CC} • f_{in} + I_{CC(static)}.

NL17SZ74



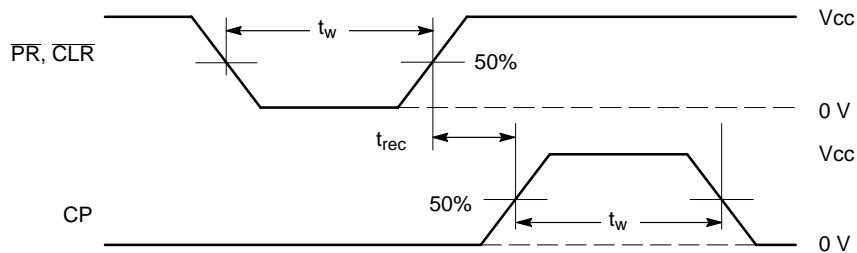
WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES

$t_R = t_F = 3.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns



WAVEFORM 2 – PROPAGATION DELAYS

$t_R = t_F = 3.0$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns



WAVEFORM 3 – RECOVERY TIME

$t_R = t_F = 3.0$ ns from 10% to 90%; $f = 1$ MHz; $t_w = 500$ ns

Output Reg: $V_{OL} \leq 0.8$ V, $V_{OH} \geq 2.0$ V

Figure 1. AC Waveforms

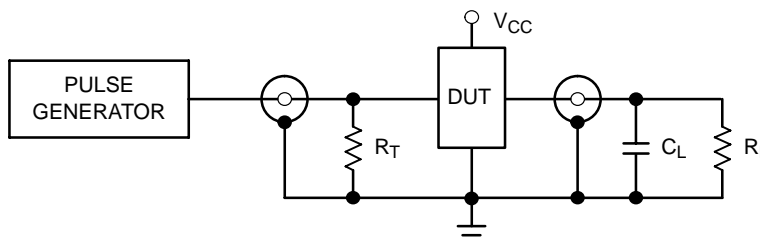
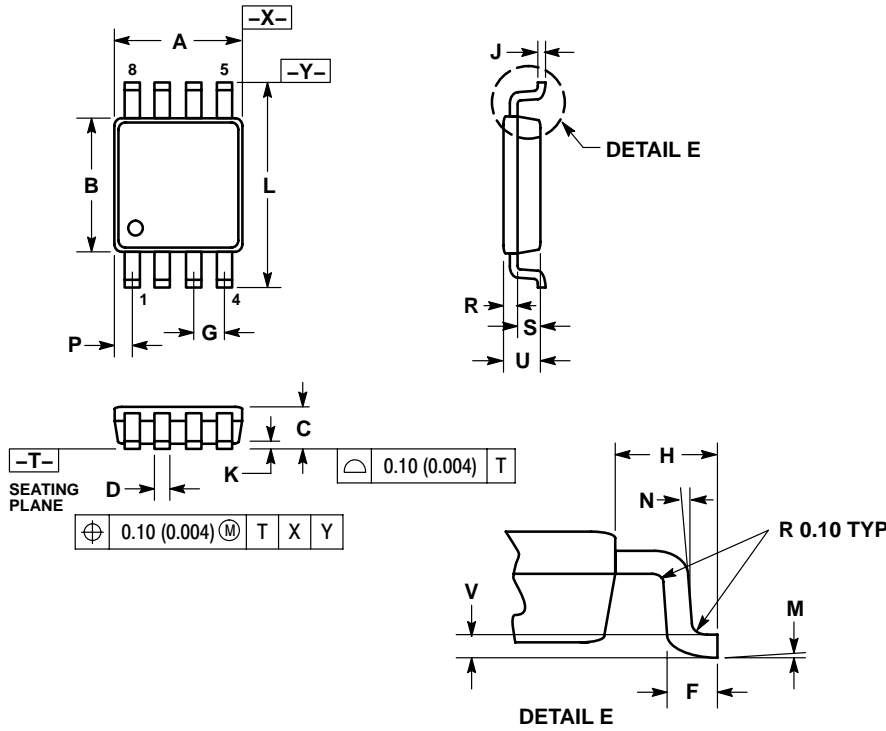


Figure 2. Test Circuit

NL17SZ74

PACKAGE DIMENSIONS

US8
US SUFFIX
CASE 493-02
ISSUE B

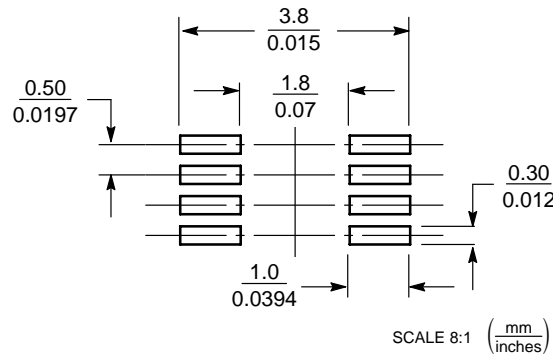


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION "A" DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR. MOLD FLASH, PROTRUSION AND GATE BURR SHALL NOT EXCEED 0.140 MM (0.0055") PER SIDE.
4. DIMENSION "B" DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION. INTER-LEAD FLASH AND PROTRUSION SHALL NOT EXCEED 0.140 (0.0055") PER SIDE.
5. LEAD FINISH IS SOLDER PLATING WITH THICKNESS OF 0.0076-0.0203 MM. (300-800 °).
6. ALL TOLERANCE UNLESS OTHERWISE SPECIFIED ±0.0508 (0.0002").

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.90	2.10	0.075	0.083
B	2.20	2.40	0.087	0.094
C	0.60	0.90	0.024	0.035
D	0.17	0.25	0.007	0.010
F	0.20	0.35	0.008	0.014
G	0.50 BSC		0.020 BSC	
H	0.40 REF		0.016 REF	
J	0.10	0.18	0.004	0.007
K	0.00	0.10	0.000	0.004
L	3.00	3.20	0.118	0.126
M	0°	6°	0°	6°
N	5°	10°	5°	10°
P	0.23	0.34	0.010	0.013
R	0.23	0.33	0.009	0.013
S	0.37	0.47	0.015	0.019
U	0.60	0.80	0.024	0.031
V	0.12 BSC		0.005 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.